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INS. A1

STM SWITCHING ARRANGEMENT

The proposed Broadband - Integrated Services Digital Network (B-ISDN) requires switching of data using the Asynchronous Transfer Mode (ATM) multiplex structure, with all services placed in cells of 53 octets including routing information.

Ins A2 The existing network employs Synchronous Transfer Mode (STM) to carry individual octets along predetermined routes, controlled by stores in the switches.

For these reasons there are three possible strategies for the introduction of ATM based B-ISDN alongside the current STM network:

1) Overlay network.

The addition of an ATM network alongside the existing STM network. B-ISDN services are carried on the overlay, and existing services remain on the STM.

This solution requires major capital investment to introduce ATM at a national level, and there is no guarantee that the service take-up will be sufficient to cover this cost within a reasonable time. This also limits

2

the flexibility of management of the network.

2) Emulation over ATM.

ATM can provide a "circuit emulation" of an STM circuit, and this is often seen as the way to support STM services on an ATM network.

It has been assumed that the existing STM services (e.g. voice) can eventually be carried over the ATM network by adapting the service into the ATM cells. This produces delays for packetisation, and also requires the STM service to be resilient against cell loss, which many services (notably H.261 video) are not yet able to cope with.

Therefore, while this may be possible when ATM is a more mature environment, the services are not yet sufficiently developed to use ATM.

3) Dual mode network.

An arrangement which provides the ability to switch both ATM traffic and STM traffic in the same switch fabric. This avoids the problems above, and has other benefits as well. Accordingly, it is required to make it possible.

INS A3 >

According to the present invention there is provided an STM telecommunications switch comprising a plurality of parallel data switching planes and a parallel control plane, each plane having an equal number of input ports and output ports and a central switching unit to switch each input port to any output port and wherein the data is switched in octets.

The invention is of a switch, capable of switching STM traffic in a central core. There are several possible ways to implement such a switch, and one such implementation is referenced

below.

The switch provides external ports, each of which is designed to support STM (multiples of 64 kbit/s) traffic.

The switch core is formed of units capable of switching STM octets (using control stores to define the route).

The present invention may be implemented using a switch fabric generally similar to that described ~~and claimed for an ATM Switching Arrangement in United Kingdom Patent Applications Nos. 9116748.6, 9116749.4, 9116750.2, and 9116763.5 which are included herein by reference. These applications give a more detailed description of the construction and operation of the switch.~~

INS A4 ~~The present invention will now be described, by way of example, with reference to the accompanying drawings, in which :-~~

~~Figure 1 shows a schematic diagram of a switch arrangement for ATM operations; and~~ according to the prior art

~~Figure 2 shows a schematic diagram of a switch arrangement for STM operation.~~

INS A5 The concept of the switch of the present invention is to use the same switch core as has been described with reference to Figures 1 to 22B inclusive ~~in the above identified patent applications~~ for an ATM switch as an STM switch, the same interconnect and core technology being used.

This covers the basic operation of the switch for STM traffic, subsequent sections cover particular subjects in more detail.

The core of the switch described in detail ~~in the~~ above ~~identified patent applications~~ can be used as the space switch in a Time Space Time (TST) based STM switch.

The 7 data planes will be used for switching different data. In the core of the switch the central data switch acts as a simple STM switching device, using a control store for STM switching. Individual ports can operate in either the ATM or the STM mode of operation, or mixed if both functions are provided.

Changing the numbers for the switch so that the cycle time is a simple fraction of the 125 microsecond frame reduces the control store requirements significantly. Operating at a logical rate of around 40M, a cycle time of a quarter of a frame would work with 20

central stages, a cycle of a fifth of a frame (25 micro seconds) works with 16 central stages. Growth based on a factor of 16 is easier to understand and the shorter cycle time is attractive.

As an STM switch will be required to carry 10 bits of data (8 data bits, 1 for channel associated signalling, 1 for parity/checking) the capacity would be less than CLOS at these rates. There are two options available, add an eighth data plane or increase the data rate. Increasing the data rate improves ATM transmission as well, so the current design is based on a cycle of a sixth of a frame running at a data rate of 49.152M. The cycle time is at 21 microseconds.

The access units (AUs), for broadband would be different from the STM AUs. For significant cost reasons, there could be two types of STM AUs. The Access Unit-Narrow Band (AUN), which has the full 64K capability, and a much simpler subset the Access Unit-Cross-Connect (AUC) that only does Synchronous Digital Hierarchy (SDH) switching. The AUN can do SDH switching as well.

In the STM mode of operation the common core provides a space switching capability that supports SDH and 64K switching for 256 ports. The space switching uses the time domain to limit the interconnection required. Because of this use of the time domain, there is a fixed delay across the switch core this depends on the relative position of the ports but ranges from 0 to 25 microseconds. Time switching elements are required at the access units to send data to and from the switch at the appropriate times.

Figure ~~2~~ 24 shows the basic principles behind the STM operation as against the ATM operation shown in Figure ~~1~~ 23.

The core is common but is used in different ways in the two switches, while the AUs are significantly different for the two types of switches.

The description that follows is for ~~thSTM~~ the STM operation, the ATM operation having been covered in the above referenced patent applications.

The switch operates in units of 64K, so for SDH switching 9 control stores will have to be set up for each column to be switched.

To handle basic 64K data 8 switched bits are required. To be able to provide error detection and appropriate recovery it is desirable to add 1 or 2 extra bits, to carry parity and long time based checking. The core could equally handle 8, 9, or 10 bits of data for STM.

The incoming AU will timeswitch the incoming stream to one of the 7 data streams to the cores, this could be a full double buffered function for timeslot sequence integrity.

The basis of this time switch is to pass the data through the first available opportunity through the core. This timeswitch need not have a long store.

This has a similar function that takes data from the 7 data streams and generates the outgoing data. Again this can be double buffered if required.

The time switch here takes the data when delivered, and then performs the appropriate full frame time switching to deliver the data when required.